

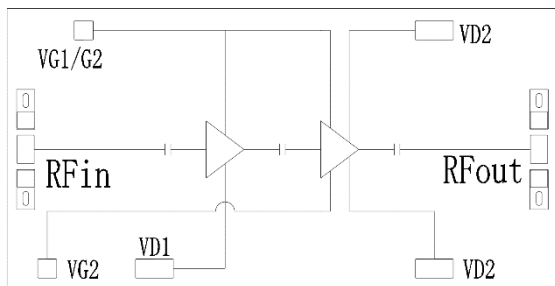
1.7 GHz-6.5 GHz | 35W | 28V | GaN MMIC PA

General Description

GNNT1765-42B is a broadband high-power amplifier chip fabricated using the GaN HEMT process, operating across a frequency range of 1.7 GHz to 6.5 GHz. The chip features dual power supply, with a typical operating voltage of $V_D = +28\text{ V}$ and $I_{DQ} = 1.5\text{ A}$. In continuous wave mode, it delivers a small signal gain of 28 dB and a saturated output power of 35 W with 40% PAE.



Block Diagram



Features

- Operating Frequencies: 1.7GHz ~6.5 GHz
- Output Power (P_{sat}): 35W (CW)
- Power Gain: 19 dB
- $DE@P_{sat}$: 40%
- Operating Voltage: 28 V
- Support CW mode
- Size: 4.2mmx2.9mmx0.1mm

Applications

- Electronic Warfare
- Test Equipment
- High frequency broadband application

Recommended Operating Conditions

Parameter	Value
Drain-Source Voltage (V_D)	28 V
Quiescent Current (I_{DQ})	1.5 A
Gate-Source Voltage (V_G)	-2.30 V (Typ)
Dynamic Drain Current (I_{DD})	3.2 A (Typ)

Note:

1. All the RF spec tested under recommended conditions.
2. Bias-up Procedure : Set V_G to the pinch-off (V_P) voltage, typically -5 V , then turn on V_D to nominal supply voltage (28V)
3. Bias-down Procedure : Turn off RF signal, then turn off V_D and wait 1 second to allow drain capacitor dissipation, turn off V_G .

Absolute Maximum Ratings

Note:

1. Operating outside the rated range may cause irreversible damage to the die

Parameter	Range Value
Drain-Source Breakdown Voltage (BV_{DS})	120 V
Drain-Source Voltage Range, (V_D)	20 to 32 V
Gate-Source Voltage Range, (V_G)	-10 to +1 V
DC Power Consumption (P_D)	80 W
Operating Temperature Range (T_W)	-55 to 85 °C
Storage Temperature Range (T_{STG})	-55 to 175 °C
Channel Junction temperature (T_{CH})	225 °C
Sintering temperature (T_M)	310 °C
Maximum Input Power, CW (P_{in}), $T_A = 25^\circ\text{C}$	30 dBm
Output (VSWR)	$\geq 3:1$ ($V_D=28\text{V}$, $T_W=85^\circ\text{C}$, $P_{in}=27\text{dBm}$, arbitrary phase)
	$\geq 10:1$ ($V_D=20\text{V}$, $T_W=85^\circ\text{C}$, $P_{in}=27\text{dBm}$, arbitrary phase)

RF Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency	1.7	-	6.5	GHz
G_{LIN}	Linear Gain	26	-	-	dB
ΔG_{sat}	Psat Gain Flatness	-	± 1.5	-	dB
P_{sat}	Output Power	45	-	-	dBm
PAE_{sat}	Saturation additional efficiency	36	-	-	%
RL_{IN}	Input Return Loss	-12	-	-	dB
RL_{OUT}	Output Return Loss	-12	-	-	dB
Harmonic	Harmonic	-	-	-12	dBc

Note:

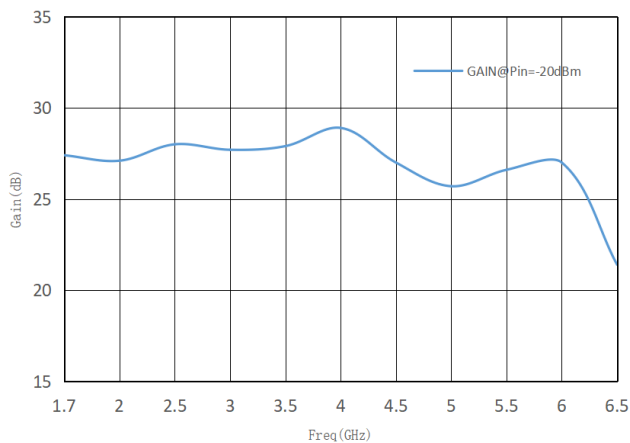
1. Test condition: $T_A = 25^\circ\text{C}$, $V_D = 28\text{V}$, $IDQ = 1.5\text{A}$, CW

Typical RF Test Data Graphic ($V_D=28\text{ V}$, $I_{DQ}=1.5\text{ A}$)

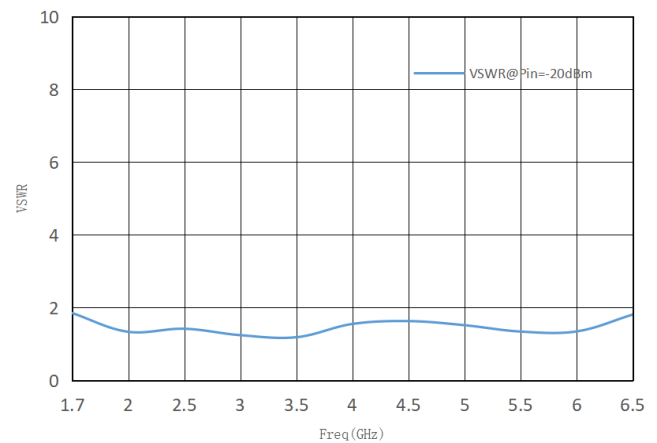
Note:

1.All the test condition: $T_A = 25\text{ }^{\circ}\text{C}$, $V_D = 28\text{ V}$, $I_{DQ} = 1.5\text{ A}$, CW

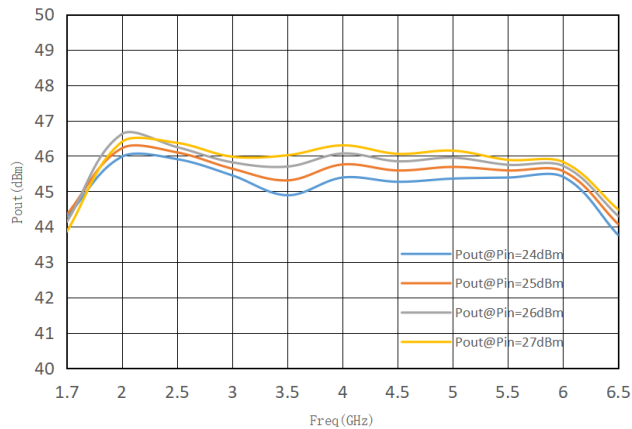
Small signal gain S21



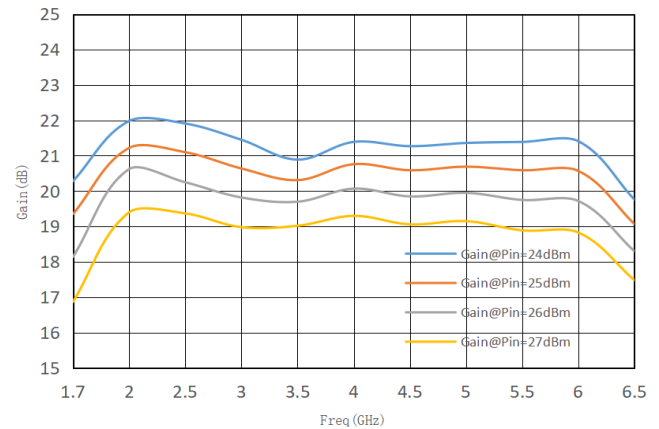
Input VSWR



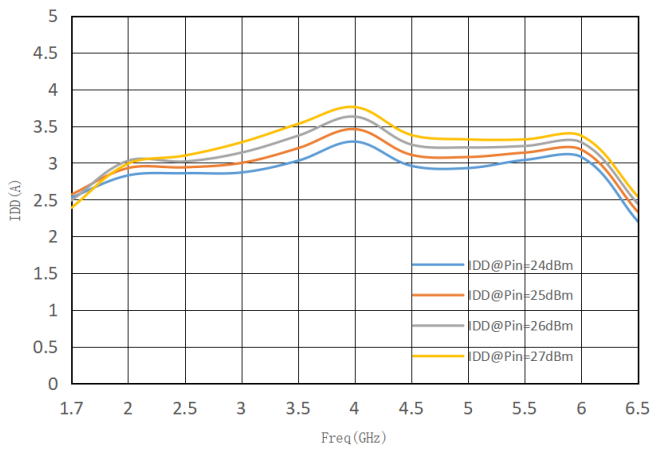
Output Power vs. Input Power



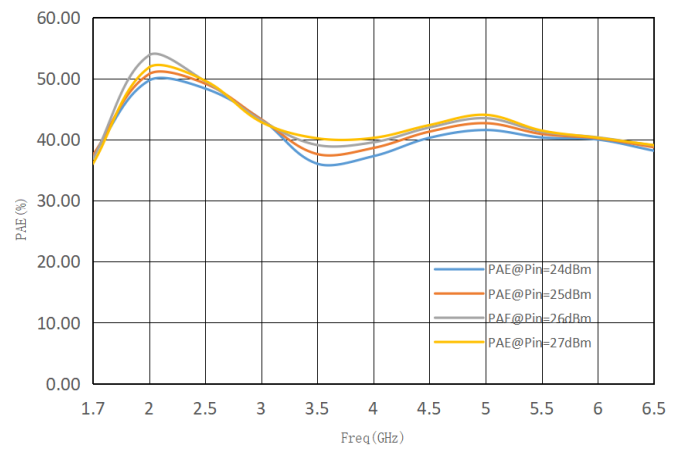
Power Gain vs. Input Power



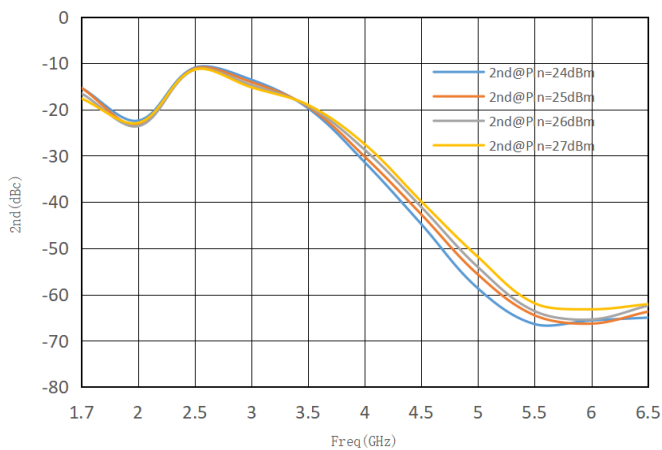
Drain current vs. Input Power



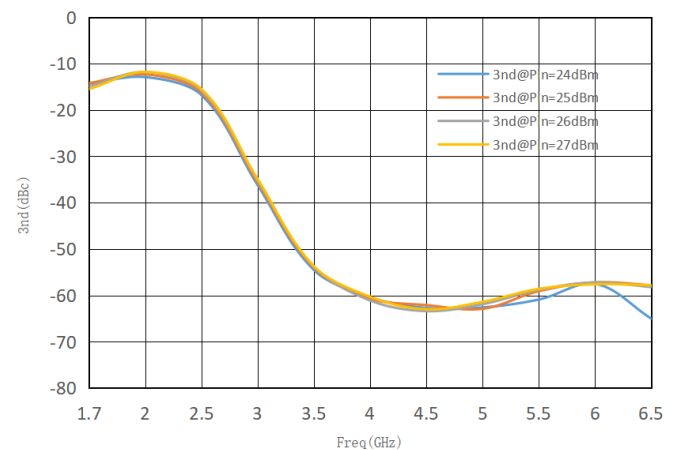
PAE vs. Input Power



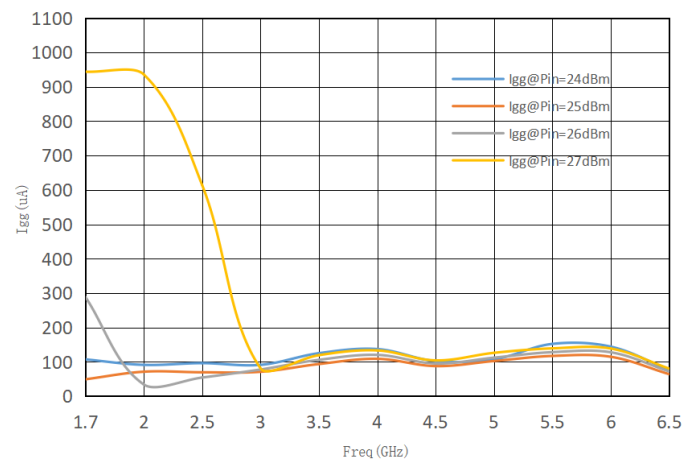
2nd harmonic vs. Input power



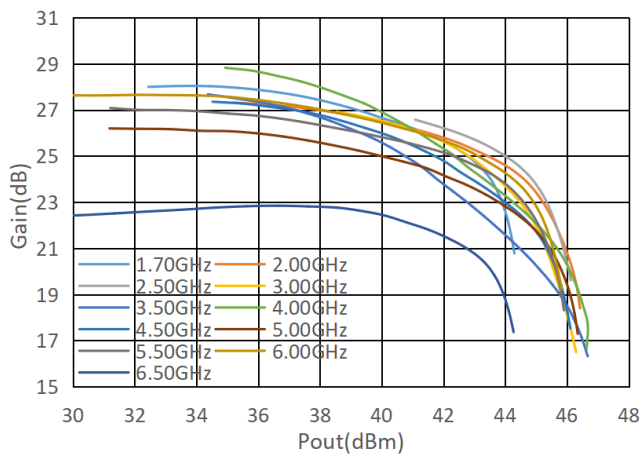
3rd harmonic vs. Input power



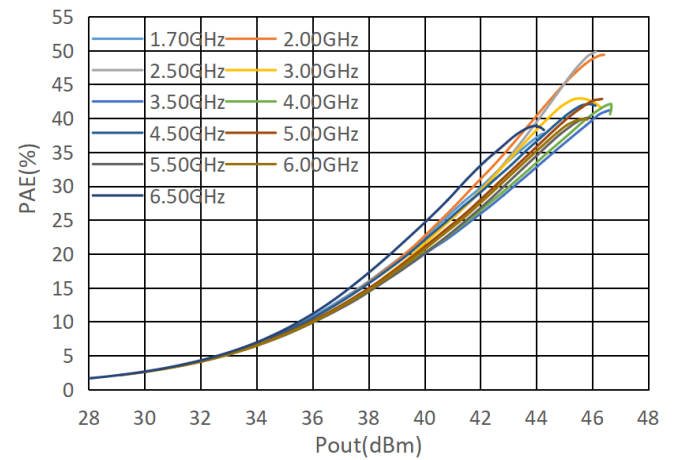
Gate current vs. Input power



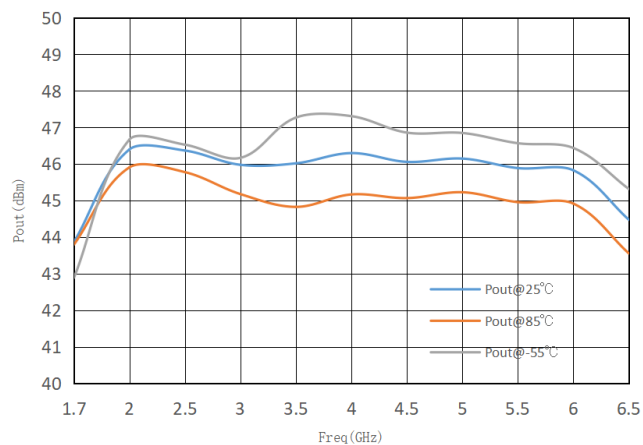
Pout vs. Gain Over Frequency



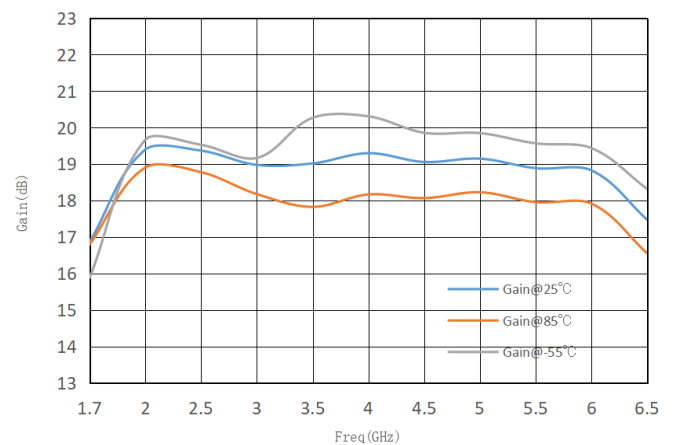
PAE vs. Pout Over Frequency



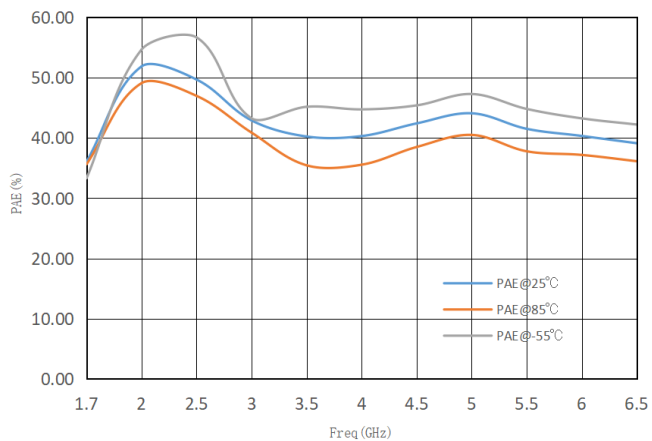
Pout vs. Frequency Over temperatures



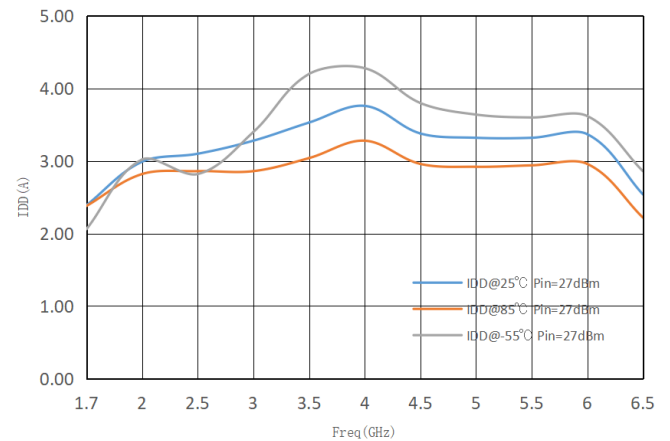
Power Gain vs. Temperatures vs. Freq



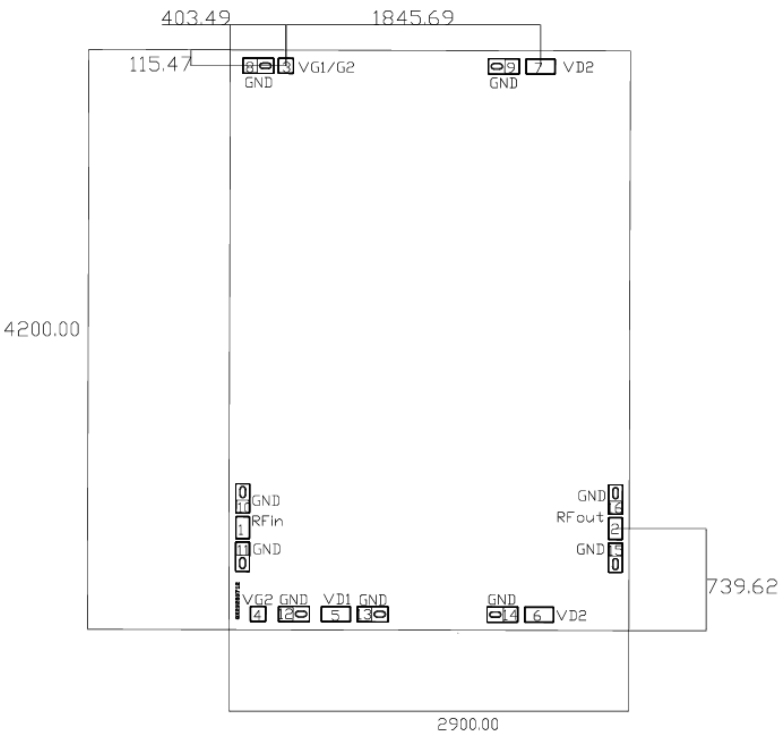
PAE vs. Freq Over Temperatures



Drain current vs. Temperatures



Mechanical Information

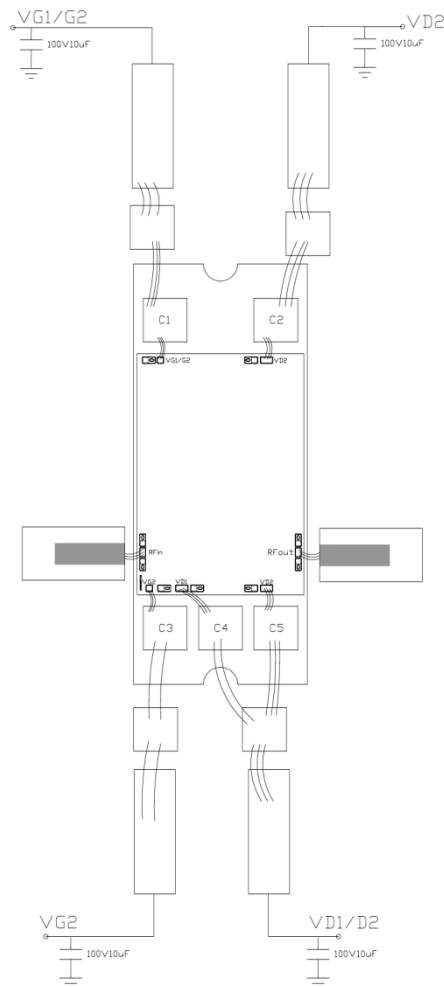


- Note:
- 1. All dimension tolerances are +/- 0.10 or +/-0.20 μm.
 - 2. This package is lead-free/RoHS compliant.

Bonding PIN Definition

PIN	Symbol	Description
1	RFin	RF signal input with an external 50Ω system and built-in DC Block function
2	RFout	RF signal output with an external 50Ω system and built-in DC Block function
3	VG1/G2	Gate negative voltage Supply: 1/Supply 2
4	VG2	Gate negative voltage Supply 2
5	VD1	Drain + 28 V voltage Supply 1
6、 7	VD2	Drain + 28 V voltage Supply 2
8-16	GND	Connect to Ground

Reference Design Circuit



Note:

1. It is recommended to use molybdenum-copper as the substrate for chips, with a preference for gold-tin eutectic alloy to ensure proper grounding.
2. The RF port is constructed using three gold wires with a diameter of 25 μm bonded together, and the RF microstrip line is positioned as close as possible to the chip's input and output RF ports.
3. Pay attention to heat dissipation design to prevent excessive chip junction temperature; during ensure the surface temperature of the substrate does not exceed 85°C.
4. This product is electrostatic-sensitive; take anti-static precautions during use and assembly by wearing an anti-static grounding bracelet and ensuring proper grounding of the sintering and bonding stations.
5. For external capacitors, a capacitor with a nominal capacitance of 1200 PF is recommended. The distance between the capacitor and the chip should be as small as possible; additionally, a 1.2 nF filter capacitor must be connected externally to the Gate and Drain.



This product is highly sensitive to static electricity!

Revision History

Data	Revision	Datasheet Status
2023/09/01	Rev 1.0	Preliminary Datasheet
2023/09/16	Rev 1.1	Add 32V data
2023/11/17	Rev 1.2	Update 28V & 32V data
2024/01/13	Rev 1.3	Deleta 32V data, Update 28V data
2025/03/28	Rev 1.4	Add VSWR data