

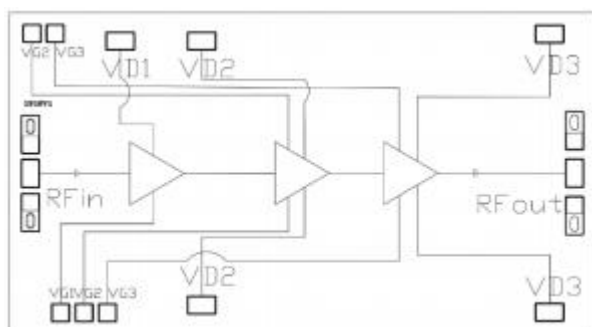
13 GHz-17 GHz | 16W | 28V | GaN MMIC RF PA

General Description

GNNT130170-42B is a broadband high-power amplifier chip fabricated using the GaN HEMT process, operating across a frequency range of 13 GHz to 17 GHz. The chip features dual power supply, with a typical operating voltage of $V_D = +28\text{ V}$ and $I_{DQ} = 230\text{ mA}$. In continuous wave mode, it delivers a small signal gain of 27 dB and a saturated output power of 16 W with 38% PAE.



Block Diagram



Applications

- Radar
- Electronic Warfare
- Test Equipment
- High frequency broadband applications

Recommended Operating Conditions

Parameters	Value
Drain-Source Voltage (V_D)	28 V
Quiescent Current (I_{DQ})	230 mA
Gate-Source Voltage (V_{G1})	-2.55 V (TYP)
Gate-Source Voltage (V_{G2}, V_{G3})	-2.53V (TYP)
Dynamic Drain Current (I_{DB})	1.5 A (TYP)

Note:

1. All the RF spec tested under recommended conditions.
2. Bias-up Procedure: Set VG to the pinch-off (VP) voltage, typically -5 V, then turn on VD to nominal supply voltage (28V)
3. Bias-down Procedure: Turn off RF signal, then turn off VD and wait 1 second to allow drain capacitor dissipation, turn off VG

Features

- Operating Frequencies: 13 GHz ~17 GHz
- Output Power (P_{sat}): 16W
- Power Gain: 22 dB
- D E: 38%
- Operating Voltage: 28 V
- Support CW & Pulse mode
- Size: 1.8mmx3.3mmx0.1mm

Absolute Maximum Ratings

Note:

1. Operating outside the rated range may cause irreversible damage to the die

Parameters	Range Value
Drain-Source Breakdown Voltage (BV_{DS})	120 V
Drain-Source Voltage Range, (V_D)	20 to 32 V
Gate-Source Voltage Range, (V_G)	-10 to +1 V
DC Power Consumption (P_D)	150 W
Operating Temperature Range (T_W)	-40 to 85 °C
Storage Temperature Range (T_{STG})	-65 to 150 °C
Channel Junction temperature (T_{CH})	225 °C
Sintering temperature (T_M)	310 °C
Maximum Input Power, CW (P_{in}), $T_A = 25^\circ\text{C}$ (P_{in})	30 dBm

RF Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency	13		17	GHz
G_{LIN}	Linear Gain	-	22	-	dB
ΔG_{sat}	Psat Gain Flatness	-	± 1	-	dB
P_{sat}	Output Power	-	42	-	dBm
PAE_{sat}	Saturation additional efficiency	-	38	-	%
RL_{IN}	Input Return Loss	-11	-	-	dB
RL_{OUT}	Output Return Loss	-4	-	-	dB
Harmonic	Harmonic	-40	-	-	dBc

Note:

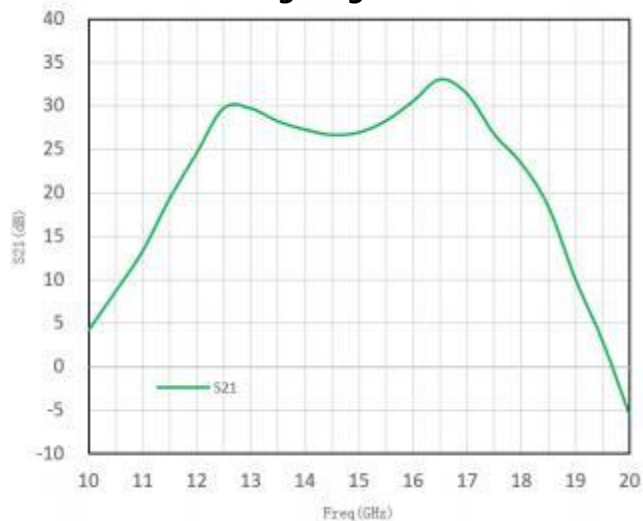
1. Test condition: $T_A = 25^\circ\text{C}$, $V_D = 28\text{V}$, $I_{DQ} = 230\text{ mA}$, CW

Typical RF Test Data Graphic ($V_D=28\text{ V}$, $I_{DQ}=230\text{ mA}$)

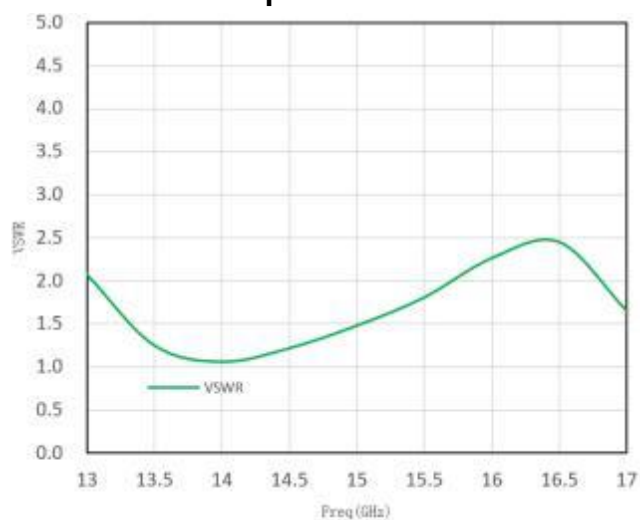
Note:

1.All the test condition: $T_A = 25\text{ }^{\circ}\text{C}$, $V_D = 28\text{ V}$, $I_{DQ} = 230\text{ mA}$, CW

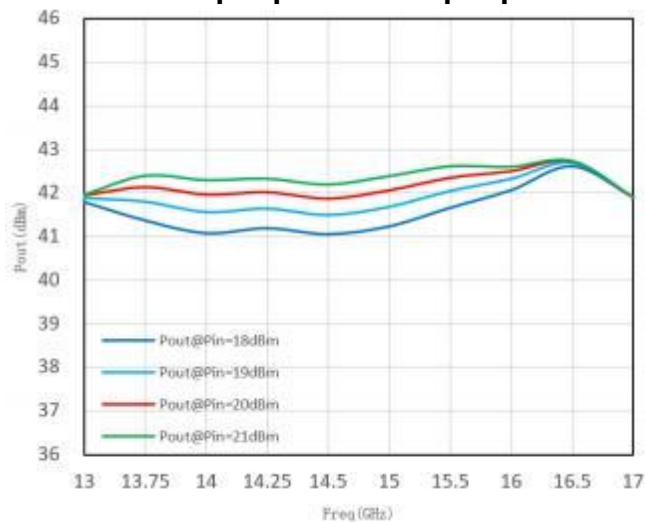
Small signal gain S21



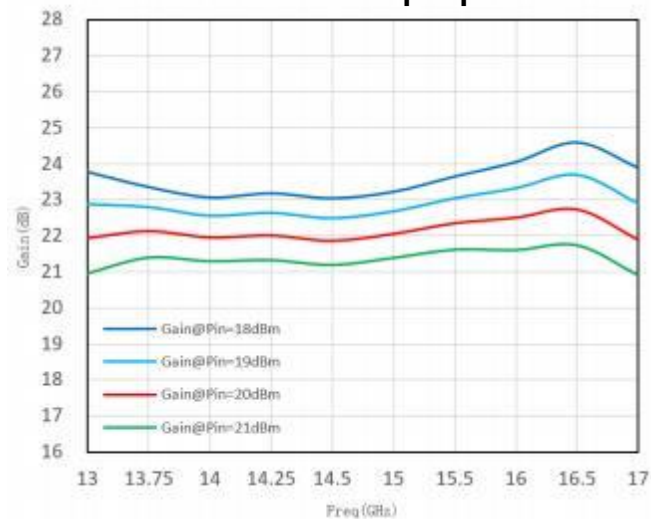
Input VSWR



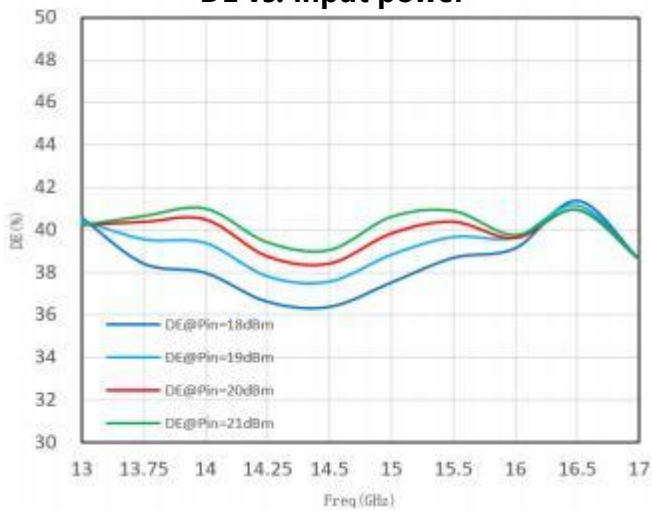
Output power vs. Input power



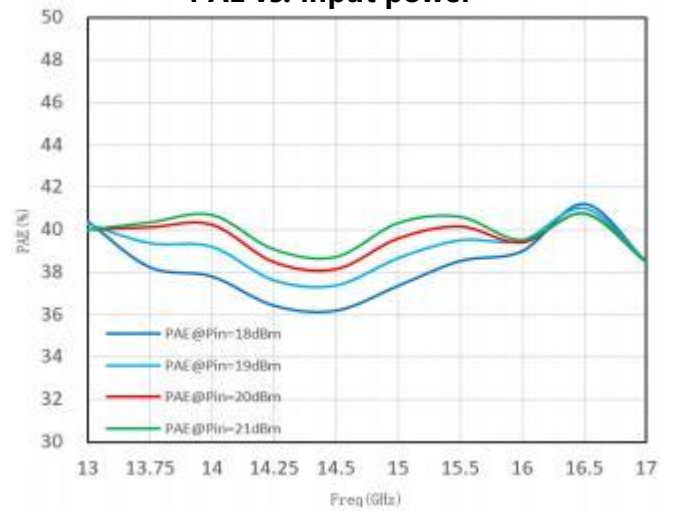
Power Gain vs. Input power



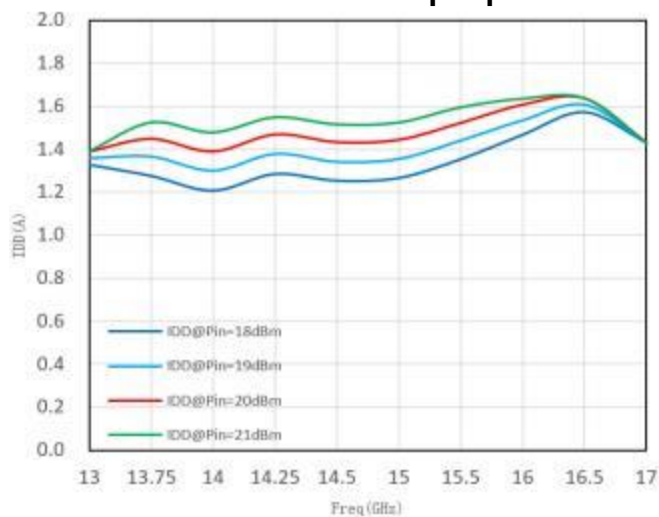
DE vs. Input power



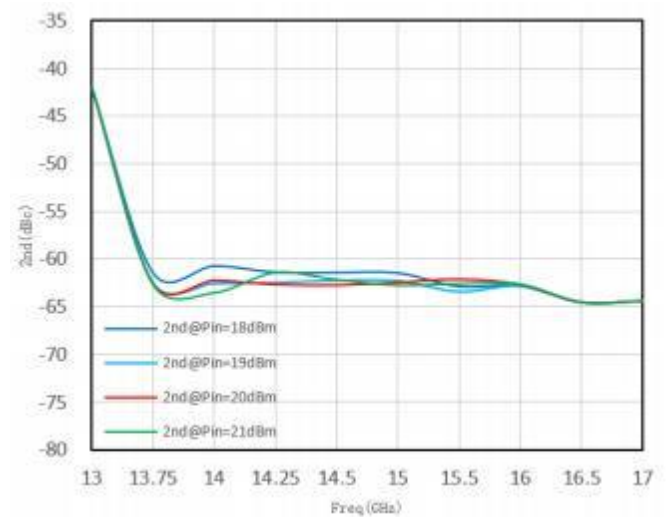
PAE vs. Input power



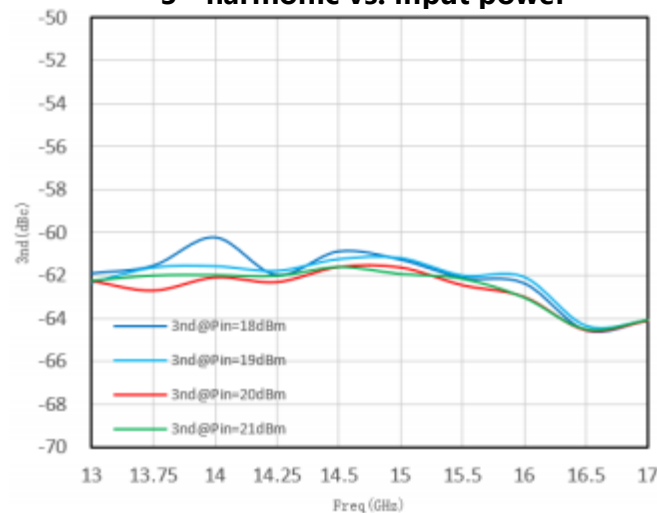
Drain current vs. Input power



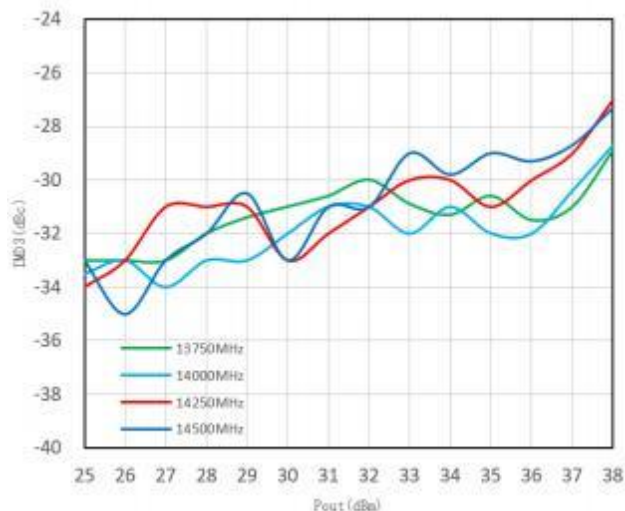
2nd harmonic vs. Input power



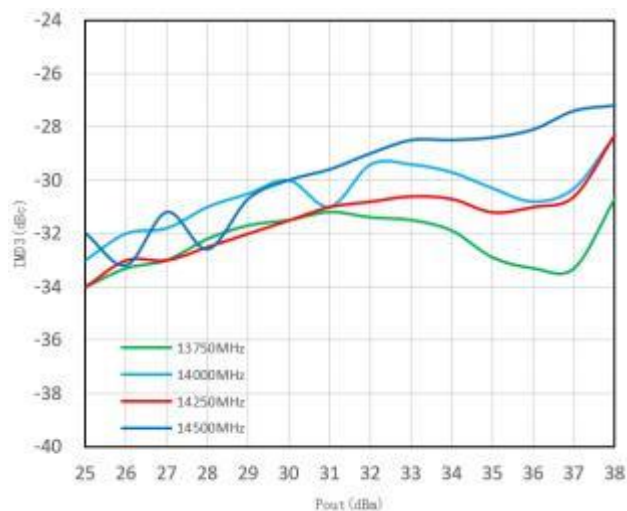
3rd harmonic vs. Input power



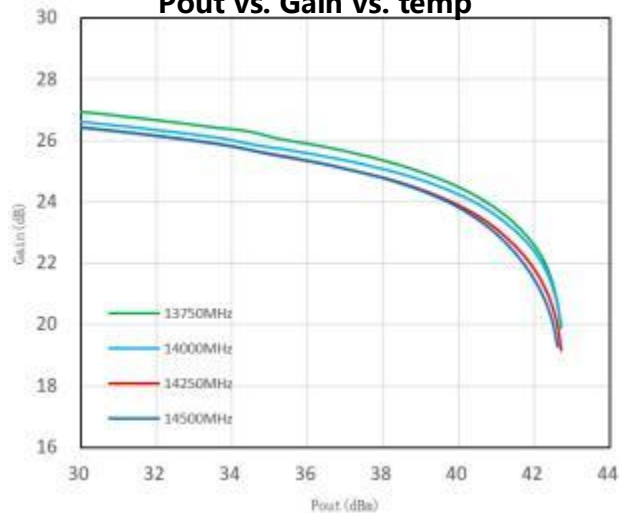
Third-order intermodulation @ signal frequency of 5 MHz



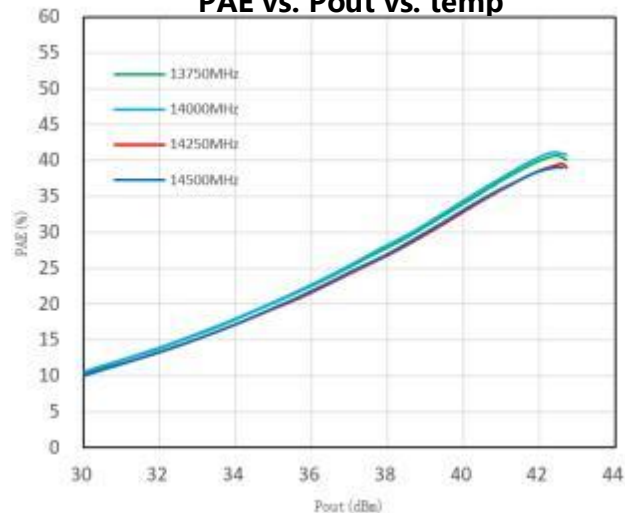
Third-order intermodulation @ signal frequency of 20 MHz



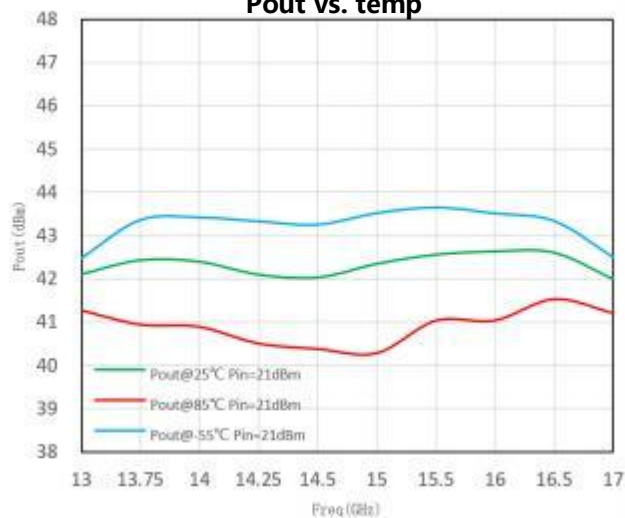
Pout vs. Gain vs. temp



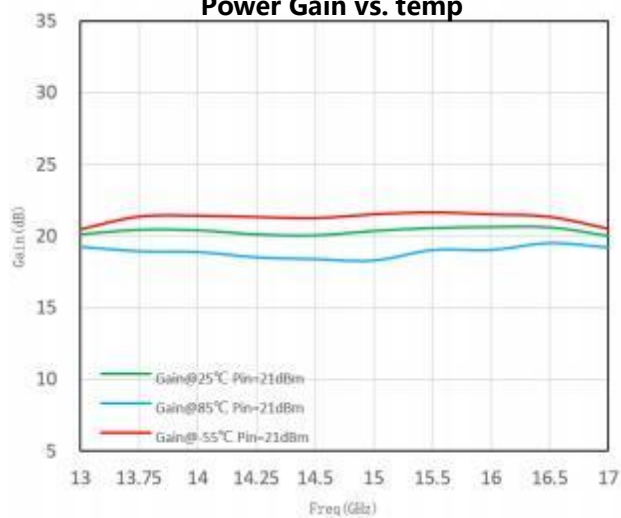
PAE vs. Pout vs. temp



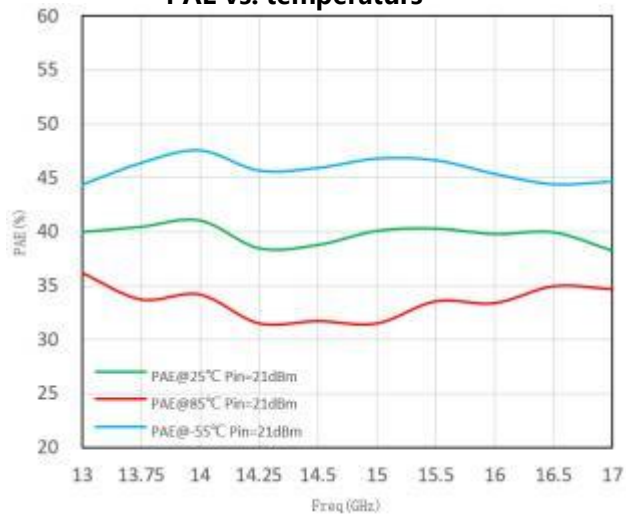
Pout vs. temp



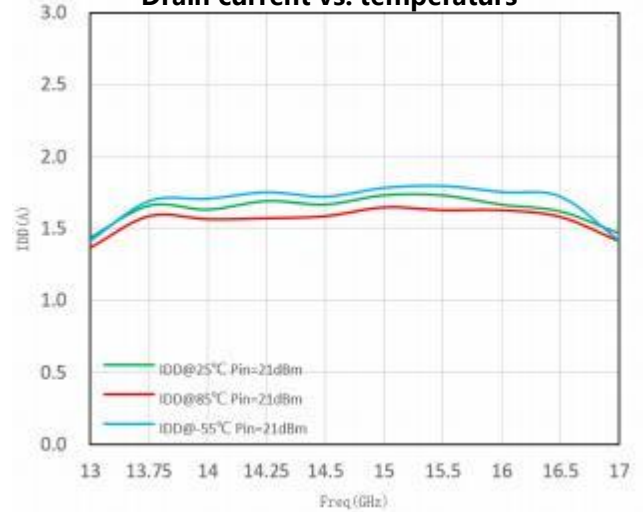
Power Gain vs. temp



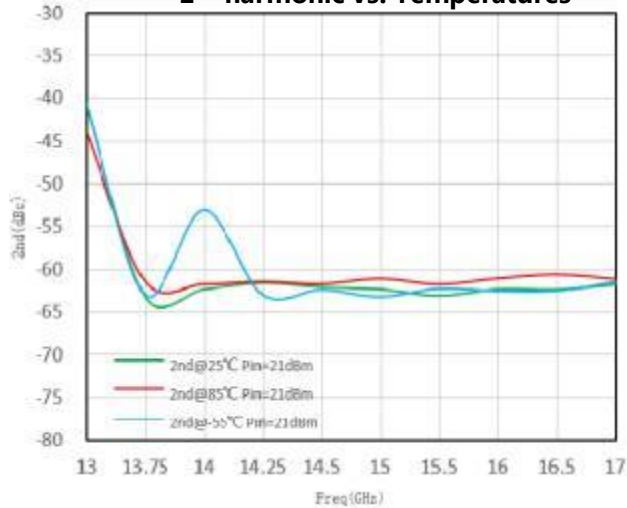
PAE vs. temperatur



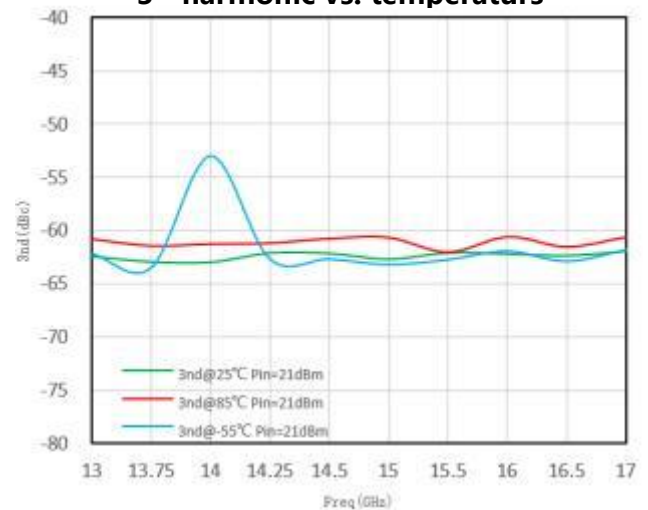
Drain current vs. temperatur



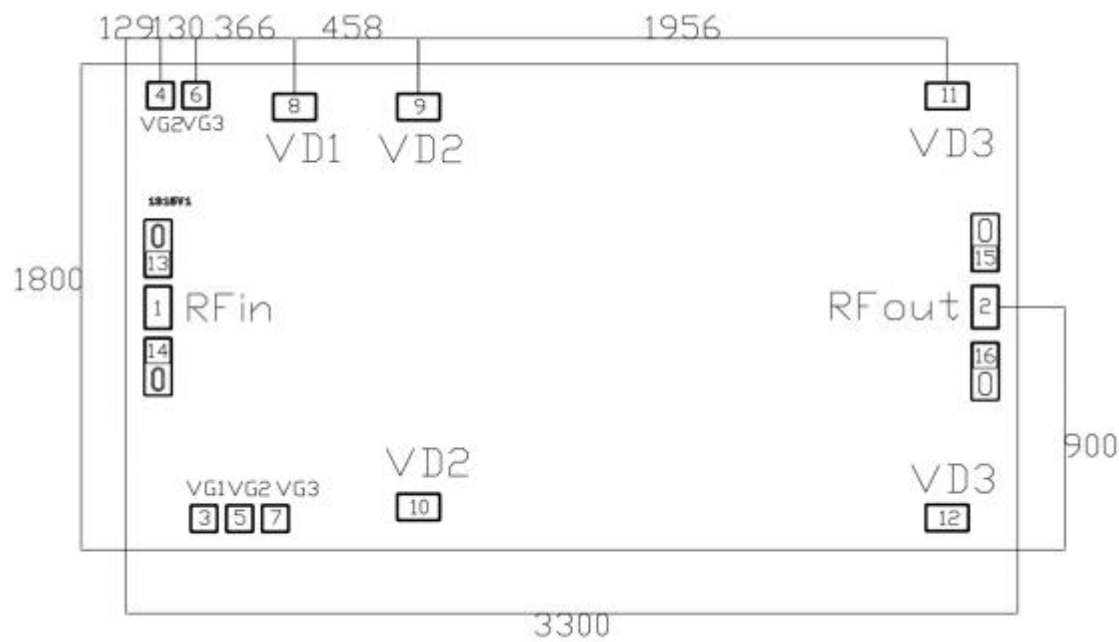
2nd harmonic vs. Temperatures



3rd harmonic vs. temperatur



Mechanical Information



Note:

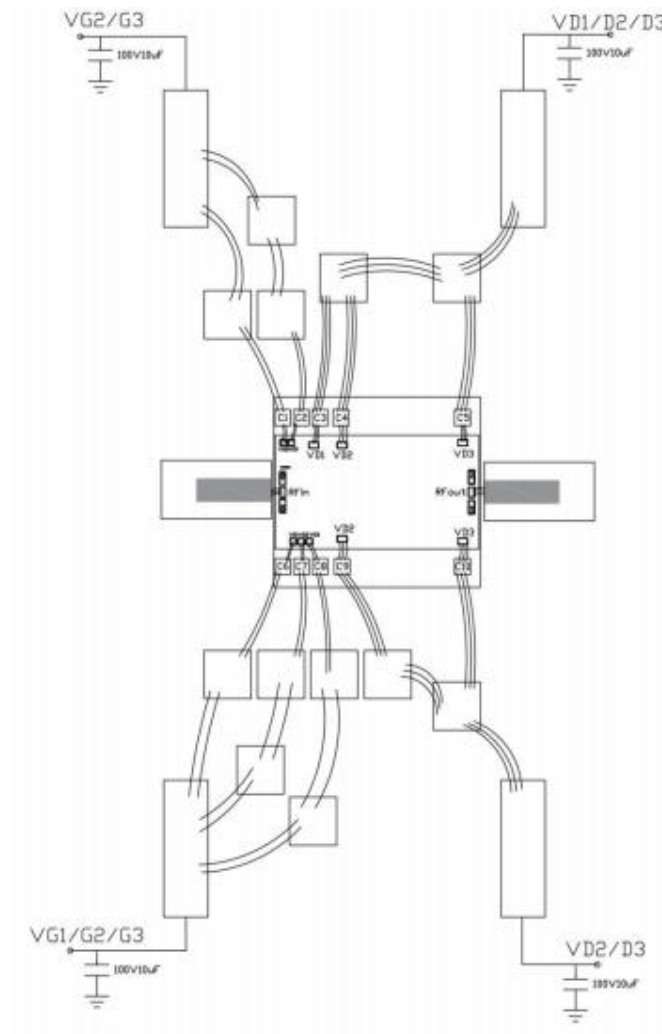
1. All dimension tolerances are +/- 0.10 or +/-0.20 um.

This package is lead-free/RoHS compliant.

Bonding PIN Definition

PIN	Symbol	Description
1	RFin	RF signal input with an external 50Ω system and built-in DC Block function
2	RFout	RF signal output with an external 50Ω system and built-in DC Block function
3	VG1	Gate negative voltage Supply: 1
4、5	VG2	Gate negative voltage Supply: 2
6、7	VG3	Gate negative voltage Supply: 3
8	VD1	Drain + 28 V voltage Supply 1
9、10	VD2	Drain + 28 V voltage Supply 2
11、12	VD3	Drain + 28 V voltage Supply 3
13-16	GND	Connect to Ground

Reference Design Circuit



Note:

1. It is recommended to use molybdenum-copper as the substrate for chips, with a preference for gold-tin eutectic alloy to ensure proper grounding.
2. The RF port is constructed using three gold wires with a diameter of 25 μm bonded together, and the RF microstrip line is positioned as close as possible to the chip's input and output RF ports.
3. Pay attention to heat dissipation design to prevent excessive chip junction temperature; during ensure the surface temperature of the substrate does not exceed 85°C.
4. This product is electrostatic-sensitive; take anti-static precautions during use and assembly by wearing an anti-static grounding bracelet and ensuring proper grounding of the sintering and bonding stations.

For external capacitors, a capacitor with a nominal capacitance of 1200 PF is recommended. The distance between the capacitor and the chip should be as small as possible; additionally, a 1.2 nF filter capacitor must be connected externally to the Gate and Drain.



**This product is
highly sensitive
to static**

Revision History

Data	Revision	Status
2024/01/30	1.0	Preliminary Datasheet